operational amplifier 39 are connected via lines 45a, 45b to a node 46a, 46b which is connected to a first programmable resistor circuit 48a, 48b via a line 47a, 47b.

The first programmable resistor circuits 48a, 48b are connected via a line 49a, 49b to the signal input 38a, 38b of the operational amplifier 39 of fully differential construction. The resistor circuits 48a, 48b each contain a plurality of parallel-connected resistors with associated controllable switches which are connected to the control input 18 of the echo cancellation filter 14 and are controlled by the DSP processor 21.

The output resistors 43a, 43b of the operational amplifier 39 are connected to second programmable resistor circuits 51a, 51b via lines 50a, 50b. The resistor circuits 51a, 51b likewise contain parallel-connected resistors with associated controllable switches which are connected to the control terminal 18 of the echo cancellation filter 14. The second programmable resistor circuits 51a, 51b are connected via lines 52a, 52b to nodes 53a, 53b, which are connected to the signal output 15a, 15b of the echo cancellation filter 14 via lines 54a, 54b.

The echo cancellation filter 14 furthermore contains third programmable resistor circuits 55a, 55b. The programmable resistor circuits 55a, 55b are connected to the node 46a, 46b via lines 56a, 56b and to the node 53a, 53b via lines 57a, 57b.

The echo cancellation filter 14 furthermore has a capacitor 58, which, in the embodiment illustrated in figure 3, is externally connected to the echo cancellation filter 14 via terminals 59a, 59b. The capacitor terminals 59a, 59b are connected via lines

60a, 60b to nodes 61a, 61b between the output resistor 43a, 43b, of the operational amplifier 39 and the second programmable resistor circuit 51a, 51b. The capacitor 58 is preferably fitted on a circuit board of the transceiver 1 using SMD technology (SMD: Surface Mounted Device). The capacitor 58 is connected to the relatively low-impedance signal nodes 61a, 61b of the echo cancellation filter 14 and is not connected to a high-impedance virtual reference potential. It is possible for the capacitor 58 to be externally connected via the capacitor terminals 59a, 59b without the electromagnetic compatibility EMC of the echo cancellation filter 14 decreasing. The implementation of the capacitor 58 as an SMD capacitor means that the capacitor 58 has a very small chip area. By way of example, the capacitor area of an SMD capacitor 58 is about 2-3 mm^2 given a capacitance of up to 10 nF. In an alternative embodiment, the capacitor 58 is integrated internally in the echo cancellation filter 14. The area requirement is larger in this case, lying above 10 mm^2 given a capacitance of about 10 nF.

Figure 4 shows the circuitry construction of a programmable resistor circuit 62, as is contained as resistor circuit 48a, 48b, 51a, 51b, 55a, 55b in the echo cancellation filter 14 according to the invention which is illustrated in figure 3.

The programmable resistor circuit 62 illustrated in figure 4 has a first terminal 63 and a second terminal 64. N resistors 65-1 to 65-n are connected to the first terminal 63 in parallel. Associated controllable switches 66 are respectively connected in series with the resistors 65. The controllable switches 66 are preferably controllable MOSFET transistors. The controllable switches each have a control terminal 67 connected to the control input 18 of the echo cancellation filter 14. The controllable switches 66

are switched under the control of the DSP processor 21. The controllable switches 66 each have a first terminal 68, connected to the associated resistor 65, and a second terminal 69 connected to the terminal 64. In this case the terminal 64 of all the programmable resistor circuits 62 contained in the echo cancellation filter 14 is connected to a virtual reference voltage terminal with a low voltage swing, with the result that the signal distortions occurring at the controllable switches 66 are minimal.

The controllable switches 66 of the first programmable resistor circuits 48a, 48b are connected to the virtual signal inputs 38a, 38b of the operational amplifier 39, as can be seen from figure 3.

The controllable switches 66 of the second programmable resistor circuits 51a, 51b and the controllable switches 66 of the third programmable resistor circuit 55a, 55b are connected via the signal outputs 15a, 15b of the echo cancellation filter 14 and via the lines 16a, 16b to the signal inputs 27a, 27b of the operational amplifier 28 of the automatic gain control circuit of the transceiver 1, as can be seen from figures 2 and 3. The signal inputs of the operational amplifiers 39, 28 are at very high impedance and have a voltage swing of almost zero, since they form a virtual ground.

The operational amplifier 39 illustrated in figure 3 forms an active input stage for impedance decoupling of the echo cancellation filter from the signal matching circuit 11 connected upstream. On account of the impedance decoupling, the required algorithm that is executed in the DSP processor 21 and serves for dynamically matching the switch positions after a connection has been set up in the training phase of the transceiver 1 is relatively simple. The echo